A 17 GHz Linear 50 Ω Output Driver in 0.12 μm Standard CMOS

Student paper

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Abstract **This work presents the design of a monolithically integrated CMOS RF tuned output amplifier for an operating frequency of 17 GHz. The linear output amplifier consists of 2 push-pull stages working in A-Class and is processed in 1.5 V, 0.12 μm standard CMOS technology. Measurement results show that the amplifier achieves a gain of 11 dB, a 1 dB compression point of 5 dBm and a third order intercept point of 15 dBm, both referred to the output. The circuit consumes 80 mA DC current at a supply voltage of 1.5 V**

I. Introduction

The growth of the wireless communication market has resulted in a tremendous amount of research on developing high-performance RF-circuits. A major challenge for chip designers is to integrate a transceiver in a single chip solution. Most commercial products are realized in BiCMOS technology, but also complete solutions in CMOS for UMTS or WLAN already exist [1], [2], and even at 24 GHz a frontend has been proposed [3]. Due to the low voltage and low gain of the CMOS transistor, the integration of a complete transceiver with acceptable performance is definitely more difficult in CMOS than in BiCMOS technologies. In spite of these handicaps it is highly desirable to use pure CMOS technology because of its low cost and high flexibility.

Due to the low transconductance of MOS-transistors, the toughest building blocks to design in CMOS transceivers are LNA and output driver interfacing 50 Ω systems. This paper presents an output amplifier for a 17 GHz transceiver in the ISM (Industrial, Science and Medical)- band. This band is reserved for future wireless HIPERLAN (High Performance Radio LAN)-applications. The modulation schema used is OFDM (Orthogonal Frequency Division Multiplexing) [4]. Since the non-constant envelope of the OFDM signal it is susceptible to nonlinear distortion from the output amplifier, the output driver has to be very linear. The other demand on the output driver is to provide sufficient power to a 50 Ω differential load at a maximum supply voltage of 1.5 V.

II. Circuit Design

The most challenging aspects of the driver stage design are to provide sufficient gain and linear output power to a 50 Ω load. A fully differential design working in the A-Class operation mode is chosen for the realization to fulfill the demands. Figure 1 shows the circuit diagram. This topology creates virtual AC grounds for the RF signal at the power supply and ground nodes. Because of these virtual AC grounds the parasitic effects due to external bond inductances at this nodes are reduced as well as the coupling to substrate. In order to avoid problems with the low carrier mobility in PMOS transistors only NMOS transistors are used.

The whole amplifier consists of two tuned stages with separate supply voltages. Both stages work in push-pull mode . In the first stage the DC bias voltage is produced by an on-chip network which is realized with poly-resistors and metal-capacitors. The DC voltage is fixed to half the value of Vdd1. The amplifier stages are

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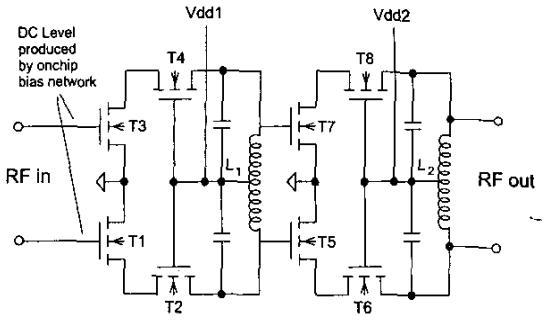

Fig. 1. Schematic of output driver without load

directly coupled, so that supply voltage of first stage is the bias voltage of the second stage. The cascode transistors (T2,T4,T6,T8) limit the voltage swing on each transistor. Without this precaution the voltage swing on the transistors (especially T5,T7) could rise up to a level of 2 times the particular supply voltage Vdd. As a consequence the transistor would have a decreased reliability and lifetime. Other advantages of using the cascode transistors are the reduced miller capacitance and the improved linearity of each stage.

Both stages are tuned to the desired frequency of 17 GHz by a LC-tank. The resonant frequency is determined by the inductor L and the total capacitance C_{tot} seen by the inductor and can be calculated by the well known thomson equation 1.

$$\omega_{res} = \frac{1}{\sqrt{LC_{tot}}} \quad (1)$$

It order to get a high quality factor in the LC-tank it is necessary to minimize C_{tot} and maximize the inductance L. Therefore the total capacitance seen by the inductor in the circuit is realized with the inherent capacitance of the coil (inner winding and to substrate) and the capacitance of the connected transistors (drain, gate). Also the parasitics of the interconnections must be considered, especially between the two stages. In order to achieve the maximal inductance the inductors are realized as cross-coupled fully differential coils which exploits the coupling factor to increase the inductance L per chip area. While the inductor L1 is designed for an improved quality factor (inductance to series resistance ratio) and high self resonance frequency, the design criteria for L2 is the current density in the coil caused by the high DC current in the second stage (35 mA in each branch) and possible ESD-currents. This implies a staggered winding scheme for the first coil as discussed in more detail in [5], and the use of wide shunt connected metal layers for the second coil. The inductors are modelled with an in-house tool based on [6], [7]. The inductor model and algorithm can be found in [8], [9]. The obtained inductance values of the coils are L_1=490 pH and L_2=660 pH.

The width of the two stacked transistors within one cascode stage are always equal. Therefore one cascode stage can be layouted as a combined transistor structure (fig. 2) similar to a dual gate transistor. This layout option minimizes the parasitic capacitances of the transistors and saves chip area.

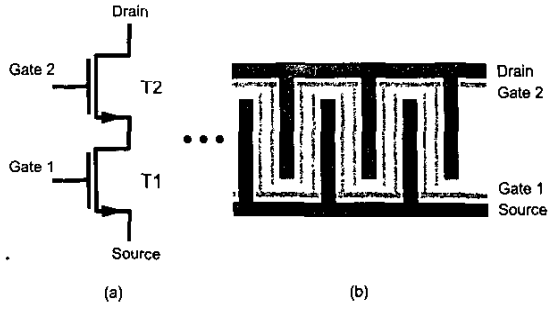

Fig. 2. (a) Cascode stage (b) equivalent layout

A special feature of the topology is the inherent ESD protection at the output provided by the coil. The low resistive inductive load at the output with a DC series resistance of only 2 Ω to the supply voltage effectively acts as a short circuit between outputs and power supply for the relatively low frequency (few MHz) ESD pulses of the human body model. Also the current density expected from possible ESD pulses is handled by the wide windings laid out for a DC-current of 35mA. Thus, the RF-outputs are protected by the power-supply ESD-protection network.

III. Experimental Results

The circuit is fabricated in a 120 μm CMOS technology with six-layer copper metallization. Figure 3 shows a micrograph of the output driver. The chip size of $0.63 \times 0.47\ mm^2$ is determined by the pad frame and not by the active area, which is only a fraction of the total chip area. Due to fill structures in all metal layers, only diffuse outlines are visible. The NMOS transistors have a cut off frequency f_T of 100 GHz and a maximum

oscillation frequency f_{max} of 50 GHz respectively [10].

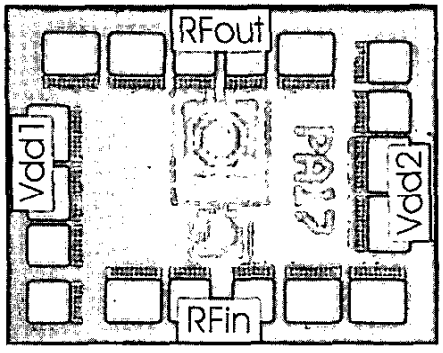

Fig. 3. Micrograph of the output driver with pad frame (size: 0.63 x 0.47 mm^2).

To evaluate the circuit performance the chip was attached on a 30x30 mm^2 0.51 mm RO4003 microwave substrate (ε_r = 3.38) with SMA connectors for input and output signals. Figure 4 shows this evaluation board mounted on a high frequency test fixture. The differential input signal was generated by a 180° hybrid coupler. Another 180° hybrid coupler was connected at the output to sum the differential output signals. DC-blocks were used at in- and output of the evaluation board.

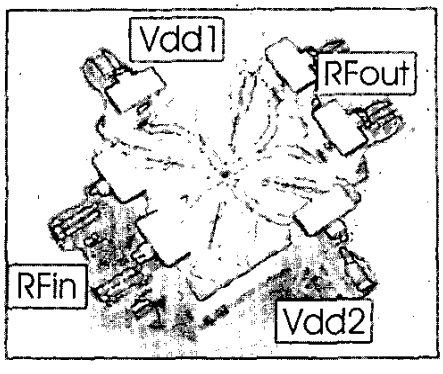

Fig. 4. Photograph of the test-board

The following measured data represent the performance of the output driver at a load of 50 Ω. They include the losses caused by the bond wires. Losses caused by the microstrip lines on the test board, RF connectors and the 180° hybrid coupler are calibrated out by the usage of an additional thru evaluation board. Input and output powers in the following figures are referred to input and output of the die (with bond wires). All measurements were performed in a 50 Ω system.

Figure 5 shows the measured power transfer characteristics at a frequency of 17 GHz. The supply voltage Vdd1 of the first stage is swept from 1.0 V to 1.2 V . The supply voltage of the second stage is fixed to voltage level of Vdd2=1.5 V. Figure 5 shows an increasing power gain with the voltage level Vdd1 up 1.2 V. No performance gain can be reached above that level. Table I gives a summary of the measured power gain, 1dB compression point and power consumption at different Vdd1 voltage levels.

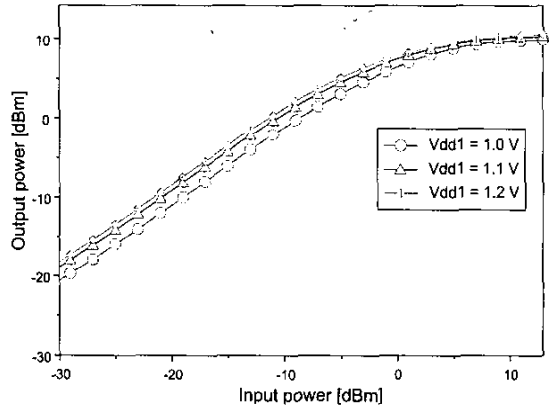

Fig. 5. Measured output power vs. input power with Vdd1 as parameter, Vdd2=1.5 V

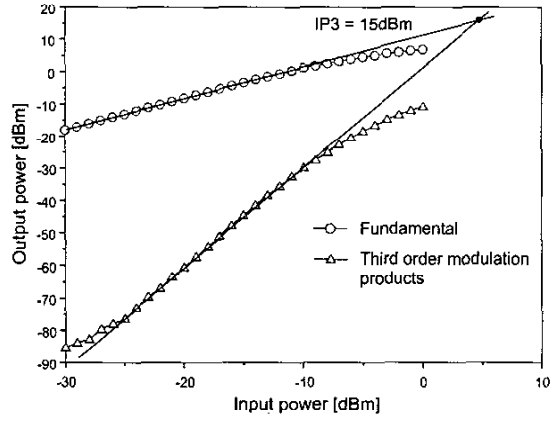

Fig. 6. Two tone measurement, 1 MHz frequency offset between the two tones

Figure 6 shows the output power of the fundamen-

tal and third order harmonic products versus the input power. The intermodulation characteristic was measured with two equal amplitude input signal tones. The first tone has a frequency of 17 GHz. The second tone is 1 MHz above at 17.001 GHz. Figure 6 gives the characteristic at Vdd1=1.2 V, the operating point were highest gain and output power were achieved. The measured intercept point third order (IP3) is at 15 dBm referred to the output. A secondary measurement with a frequency offset of 100 MHz between the two tones delivers the same result. Other IP3 points can be found in table I. At low input power levels the measured intermodulation curve differs from the ideal one. The reason for this deviation is the limiting noise floor of the spectrum analyzer. Figure 7 shows the frequency response measured with a network analyzer. The measured 3dB bandwidth is about 1 GHz.

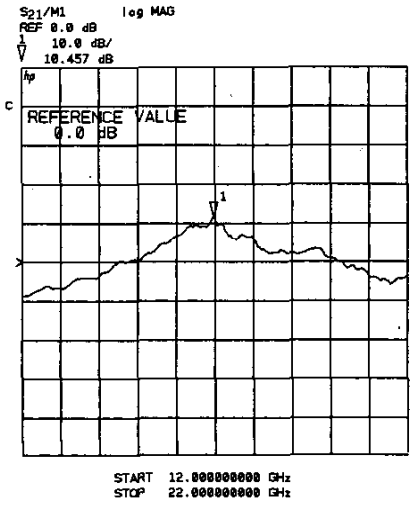

Fig. 7. Measured frequency response (input level = -20 dBm)

IV. Conclusions

A low voltage output driver for 17 GHz in a 0.12 μm CMOS technology is presented. The highly linear driver is based on a differential push-pull circuit type working in A-Class operation mode. At a voltage supply of 1.5 V the amplifiers delivers a maximal linear output power up to 5 dBm at a 50 Ω load. The small signal gain is 11 dB and IMP3 (output referred) is measured at 15 dBm. It is well-suited for future wireless LAN OFDM applications in the ISM band at 17.2 GHz.

Vdd2 [V]	1.5		
Vdd1 [V]	1.0	1.1	1.2
Power gain [dB]	9	10.5	11
1dB compression [dBm]	3	4.5	5
IP3 [dBm]	14	14	15
Idd1 [mA]	10	12	14
Idd2 [mA]	52	62	70
P_{tot} [mW]	88	106	120

TABLE I. Performance summary , 1dB compression point and IP3 referred to the output

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